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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,282	02/16/2001	Michele Borgatti	854063.616	5300

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EXAMINER	
PENDLETON, BRIAN T	
ART UNIT	PAPER NUMBER
2615	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/788,282	BORGATTI ET AL.	
	Examiner	Art Unit	
	Brian T. Pendleton	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

Applicant's arguments, see Remarks, filed 2/2/07, with respect to the rejection(s) of claim(s) 1-23 under 35 U.S.C. 102 and 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Takasu et al, US Patent 6,145,060.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters in view of Takasu et al. Walters teaches a portable audio device comprising semiconductor material 120 (see figure 5), control unit 120, microphone 46 which is part of a signal conversion unit, said unit also containing compression means, fetching means, decompression means and memory unit 122. Figure 4 shows a control unit 120 which communicates with the memory unit 122 using bus 128 (a transmission line). As taught in column 8 line 58 – column 9 line 24, voice signals from the microphone 46 are compressed by CODEC 158 and a first stream of compressed digital signals are generated to be stored in memory unit 122. Also those voice signals are decompressed by the CODEC 158 and reproduced by speaker 48. The voice circuit 152 supports the "play" function, thereby fetching the second stream of compressed signals via

CPU 120 for decompression and eventual reproduction. Memory 122 is a flash memory and thus is non-volatile. Walters does not disclose that the control unit, memory unit, signal conversion unit and transmission line are integrated in a single chip of semiconductor material. Takasu et al disclose a data storage device for storing audio data comprising microphone 23, speaker 27, a single chip of semiconductor material 1, the chip having an inherent main transmission line, non-volatile memory 25, control unit 22, encoder 24 and decoder 26 (signal conversion unit). Thus, it was well known to construct the components of a voice recording device on a single chip of semiconductor. It would have been obvious to one of ordinary skill in the art at the time of invention to consolidate the control unit, memory unit, signal conversion unit and transmission line onto one chip, as taught by Takasu, for the purpose of reducing the size of the apparatus. Per claims 2 and 3, the control unit 120 is a CPU which is a microprocessor or microcontroller.

Claims 4, 5, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters in view of Takasu as applied to claim 1 above, and further in view of Unno et al. The combination of Walters and Takasu does not disclose that the signal-conversion unit has temporary storage means coupled to a converter circuit. Inherently, Walters et al has a converter circuit in CODEC 158. The coder/decoder converts the incoming analog signal to a digital format. The use of a temporary storage means was well known in the art, as evidenced by Unno et al. Unno et al taught an audio player and recorder having a buffer memory 6 which temporarily stores data received from the compressor 4 (first stream) and data read from the flash memory 8 (second stream). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the teachings of Unno et al in the combination of Walters and Takasu and include a buffer memory after the CODEC 158. Claim 4 is met. Regarding method

claim 12, the combination reads on the claim limitations. Specifically, Walters et al has a microphone for receiving an input analog signal correlated to a voice signal, compression means for compressing the input analog signal resulting in a stream of compressed digital signals. Takasu is relied upon for the teaching of a single integrated circuit chip. Unno et al is relied upon for sending the compressed digital signals to a temporary storage means (buffer memory 6). The compressed digital signals are then sent from buffer memory to the non-volatile memory of Walters et al. During playback, a second stream of compressed digital signals are sent from non-volatile memory to the converter circuit and subsequently to decompression means 158 for decompressing the second stream and generating an output analog signal. As to claims 5 and 13, Unno et al taught that the compression means generates blocks of digital samples having a fixed dimension in column 7.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters in view of Takasu further in view of Unno as applied to claim 5 above, and further in view of Daberko. The combination of Walters et al, Takasu and Unno et al teach an apparatus comprising a semiconductor chip, bus, control unit, signal-conversion unit having a microphone, compression means, fetching means, decompression means, a non-volatile memory unit wherein the signal-conversion unit has temporary storage means coupled to a converter circuit. The combination does not teach that the temporary storage means has first and second memory buffers whereby the signal conversion unit controls transfer of digital signals alternately to the first and second memory buffers. Daberko teaches a non-volatile memory (flash) having first and second memory buffers in figure 3C. As suggested in column 9 lines 44-55, it was advantageous to allow the buffers to switch tasks. One memory buffer can be disseminated or

unloaded while the other memory buffer is written to primary memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate first and second memory buffers in the combination of Walters et al, Takasu and Unno et al. Regarding claim 7, Examiner takes Official Notice that it was well known to use RAM as memory buffers.

Claims 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al in view of Takasu further in view of Unno et al as applied to claims 5 and 12 above, and further in view of Rossum. The combination does not teach that the temporary storage means has first and second memory buffers whereby the signal conversion unit controls transfer of digital signals alternately to the first and second memory buffers and that the control means of the signal conversion unit transfers first blocks of digital signals to the first memory buffer, detects filling of the first memory buffer, transfers second blocks of digital signals to the second memory buffer and sends the first blocks to the non-volatile memory unit, detects filling of the second memory buffer and transfers third blocks of digital signals to the first memory buffer and sends the second blocks to the non-volatile memory unit. To an ordinarily skilled artisan, this feature is known as "ping-pong" buffering. The combination of Walters et al, Takasu and Unno et al while supplying a buffer, does not explicitly teach "ping-pong" buffering. However, this feature was well known in the art, as evidenced by Rossum. Column 1 lines 12-26 taught the art of ping-pong buffering noting that when a first buffer is full then a second buffer is filled and the data from the first buffer is processed. This process is repeated when the second buffer is full and control is passed back to the first buffer. Thus, there was taught alternating between two buffers and detecting filling of each of the buffers. The buffers were examined to see if they were full since control is passed to the other buffer when one is full. It would have been obvious

to one of ordinary skill in the art at the time of invention to use the feature of "ping-pong" buffering in the combination of Walters, Takasu and Unno et al.

Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al in view of Takasu and further in view of Ogawa. The combination of Walters et al and Takasu does not explicitly teach that the memory device has a first memory area storing digital signals and a second memory area containing information regarding occupation of memory locations of the first memory area. Ogawa discloses a flash EEPROM management system. The system has a flash ROM 15 having a management area and data area for storing digital signals. See figures 4 and 5a-c. As discussed in the "Summary of the Invention" section, column 2, the management area stores state information indicating whether a corresponding data area is used, unused or busy. Thus, it was well known to have a memory containing data signals and information regarding occupation (used/unused flags) of the memory locations containing data signals. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Ogawa in the invention of Walters et al and have a first memory area for data and a second memory area for data management of the data in the first memory area. Claim 9 is rejected. As to claim 10, the first sub-area is the used state flag 156 and it is inherent that another sub-area contains read-sequence pointers. Regarding claim 11, Official Notice is taken that the use and advantages of multi-level flash EEPROMS were notoriously well known in the art of digital signal storage and one of ordinary skill in the art would have been motivated to use them.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al in view Takasu further in view of Unno et al. Walters et al teach an apparatus comprising a

bus (main transmission line), control unit 120, converter circuit 158 having compression means for generating a first stream of compressed digital signals and decompression means for decompressing a second stream of compressed digital signals and generating an output analog signal, non-volatile memory unit 122 coupled to the bus for storing compressed digital signals and for generating a second stream of compressed digital signals according to control signals from control unit 120. Walters does not disclose that the control unit, memory unit, signal conversion unit and transmission line are integrated in a single chip of semiconductor material. As stated above, Takasu discloses a single chip of semiconductor having a transmission line, memory unit, control unit, and signal conversion unit (encoder/decoder). Thus, it was well known to construct voice recording devices on a single chip of semiconductor. It would have been obvious to one of ordinary skill in the art at the time of invention to consolidate the control unit, memory unit, signal conversion unit and transmission line onto one integrated chip, as taught by Takasu, for the purpose of reducing the size of the apparatus. As discussed above, it also would have been obvious to include temporary storage means in the combination of Walters et al and Takasu, per the teachings of Unno et al. Unno et al teach temporary storage means having first and second memory buffers for sequentially receiving first and second streams of compressed data for input into flash memory. As to claim 16, inherently the converter circuit 158 generates blocks of digital data for storage in the memory.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al in view of Takasu further in view of Unno et al as applied to claim 16 above, and further in view of Rossum. The combination of Walters et al, Takasu and Unno et al does not teach that the signal conversion unit controls transfer of digital signals alternately to the first and second

memory buffers and that the control means of the signal conversion unit transfers first blocks of digital signals to the first memory buffer, detects filling of the first memory buffer, transfers second blocks of digital signals to the second memory buffer and sends the first blocks to the non-volatile memory unit, detects filling of the second memory buffer and transfers third blocks of digital signals to the first memory buffer and sends the second blocks to the non-volatile memory unit. To an ordinarily skilled artisan, this feature is known as "ping-pong" buffering. The combination of Walters et al and Unno et al while supplying a buffer, does not explicitly teach "ping-pong" buffering. However, this feature was well known in the art, as evidenced by Rossum. Column 1 lines 12-26 taught the art of ping-pong buffering noting that when a first buffer is full then a second buffer is filled and the data from the first buffer is processed. This process is repeated when the second buffer is full and control is passed back to the first buffer. Thus, there was taught alternating between two buffers and detecting filling of each of the buffers. The buffers were examined to see if they were full since control is passed to the other buffer when one is full. It would have been obvious to one of ordinary skill in the art at the time of invention to use the feature of "ping-pong" buffering in the combination of Walters, Takasu and Unno et al. Claim 17 is rejected since the teaching of alternating between two buffers was suggested by Rossum. Regarding claim 18, Examiner takes Official Notice that it was well known to use RAM as memory buffers. Claim 19 is rejected since Rossum taught detecting filling of the memory buffers.

Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al in view of Takasu further in view of Unno et al, as applied to claim 15 above, further in view of Ogawa. The combination does not teach that the memory device has a first memory area

storing digital signals and a second memory area containing information regarding occupation of memory locations of the first memory area. Ogawa discloses a flash EEPROM management system. The system has a flash ROM 15 having a management area and data area for storing digital signals. See figures 4 and 5a-c. As discussed in the "Summary of the Invention" section, column 2, the management area stores state information indicating whether a corresponding data area is used, unused or busy. Thus, it was well known to have a memory containing data signals and information regarding occupation (used/unused flags) of the memory locations containing data signals. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Ogawa in the invention described by Walters et al, Takasu and Unno et al and have a first memory area for data and a second memory area for data management of the data in the first memory area. Claim 20 is met. As to claim 21, the first sub-area is the used state flag 156 and it is inherent that another sub-area contains read-sequence pointers. Regarding claim 22, Examiner takes Official Notice that it was obvious to use multi-level flash EEPROMS as they were well known in the art of digital signal storage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Pendleton whose telephone number is (571) 272-7527. The examiner can normally be reached on M-F 7-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (571) 272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brian T. Pendleton
Primary Examiner
Art Unit 2615

btp